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⑤4発明の名称　マスタスライス方式ＬＳＩの配線構造

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明　細　書

1．発明の名称

マスタスライス方式ＬＳＩの配線構造

2．特許請求の範囲

垂直方向および水平方向の配線格子が定義された第１の配線層および第２の配線層と、

これら第１の配線層および第２の配線層に定義された垂直方向および水平方向の配線格子の各格子点の対角を結ぶ斜めの配線格子が定義された第３の配線層と

を有することを特徴とするマスタスライス方式ＬＳＩの配線構造。

3．発明の詳細な説明

（産業上の利用分野）

本発明はマスタスライス方式ＬＳＩの配線構造に関し、特に配線工程以前のマスクを共通とし配線に関するマスクのみを品種ごとに設計製作してＬＳＩを作成するマスタスライス方式ＬＳＩの配線構造に関する。

（従来の技術）

従来、この種のマスタスライス方式ＬＳＩの配線構造では、すべての配線層の配線格子が垂直方向および水平方向に定義されていた（参考文献：「論理装置のＣＡＤ」，情報処理学会，昭和５６年３月２０日発行）。

いま、第２図に示すように、垂直方向格子間隔および水平方向格子間隔をともにｄとしたときに配線ネットの端子ｔ１および端子ｔ２間の配線長が高速動作を必要とするＬＳＩの遅延時間等の制約を満足するために８ｄ以内であるという制限がある場合を例にとって説明すると、端子ｔ１および端子ｔ２間を結ぶ直線の角度が０度または３０度に近いものから順に第１の配線層１および第２の配線層２を用いて配線する配線処理を行った結果、第３図に示すように、配線経路１０１と配線経路１０２とによって端子ｔ１および端子ｔ２間の配線が迂回させられ、配線長１２ｄの配線経路２０１が得られたときに、従来のマスタスライス

線経路１１１および１１２を得ることにより、制限を満たす配線長８ｄの配線経路２１１を得ていた。

（発明が解決しようとする課題）

上述した従来のマスタスライス方式ＬＳＩの配線構造では、高速動作を必要とするＬＳＩの遅延時間等の制約を満足するために設定された配線長に制限がある配線ネットの配線において配線処理後にその制限が満たされなかった場合に、制限を満たすようにするために他の配線を移動させて配線の修正を行う必要があったので、配線の修正に多大な工数を要するという欠点がある。

また、配線の修正を行っても配線長の制限を満たすことができなかった場合には、ブロックの配置修正等を行って配線処理をやり直す必要があり、さらに処理時間が増大するという欠点がある。

本発明の目的は、上述の点に鑑み、第１の配線層および第２の配線層に定義された垂直方向および水平方向の配線格子の各格子点の対角を結ぶ斜めの配線格子が定義された第３層の配線層を利用して、他の配線を移動したりブロックの配置位置を変更したりすることなしに、比較的容易に配線長の調整を行うことができるマスタスライス方式ＬＳＩの配線構造を提供することにある。

（課題を解決するための手段）

本発明のマスタスライス方式ＬＳＩの配線構造は、垂直方向および水平方向の配線格子が定義された第１の配線層および第２の配線層と、これら第１の配線層および第２の配線層に定義された垂直方向および水平方向の配線格子の各格子点の対角を結ぶ斜めの配線格子が定義された第３の配線層とを有する。

（作用）

本発明のマスタスライス方式ＬＳＩの配線構造では、第１の配線層および第２の配線層に垂直方向および水平方向の配線格子が定義され、第３の配線層に第１の配線層および第２の配線層に定義された垂直方向および水平方向の配線格子の各格子点の対角を結ぶ斜めの配線格子が定義される。

（実施例）

次に、本発明について図面を参照して詳細に説明する。

第１図は、本発明の一実施例に係るマスタスライス方式ＬＳＩの配線構造を示す図である。本実施例のマスタスライス方式ＬＳＩの配線構造は、垂直方向および水平方向の配線格子が定義された第１の配線層１および第２の配線層２と、第１の配線層１および第２の配線層２に定義された垂直方向および水平方向の配線格子の各格子点の対角を結ぶ斜めの配線格子が定義された第３の配線層３とから構成されている。

次に、このように構成された本実施例のマスタスライス方式ＬＳＩの配線構造における配線処理について、第２図～第４図を参照しながら具体的に説明する。

第２図に示すように、垂直方向格子間隔および水平方向格子間隔をともにｄとしたときに配線ネットの端子ｔ１および端子ｔ２間の配線長が高速動作を必要とするＬＳＩの遅延時間等の制約を満足するために８ｄ以内であるという制限がある場合を例にとって説明すると、端子ｔ１および端子ｔ２間を結ぶ直線の角度が０度または９０度に近いものから順に第１の配線層１および第２の配線層２を用いて配線する配線処理を行った結果、第３図に示すように、配線経路１０１と配線経路１０２とによって端子ｔ１および端子ｔ２間の配線が迂回させられ、配線長１２６の配線経路２０１が得られたときに、第４図に示すように、配線経路１０１および１０２を修正せずに、端子ｔ１および端子ｔ２の位置に第１の配線層１および第３の配線層３間のスルーホール２３１および２３２を挿設し、端子ｔ１および端子ｔ２間を第３の配線層３を用いて斜めの配線を行うことにより、制限を満たす配線長

$$\ell = \sqrt{(4d)^2 + (4d)^2} = 4\sqrt{2}\,d$$

の配線経路２２１を得ることができる。

（発明の効果）

以上説明したように本発明は、高速動作を必要とするＬＳＩの遅延時間等の制約を満足するため

に設定された配線長の制限に対して第1の配線層および第2の配線層を用いて配線処理を行った後に制限を満たしていない配線を制限を満たすようにするために第3層の配線層を利用することにより、他の配線を移動したりブロックの配置位置を変更したりすることなしに、比較的容易に配線長の調整を行うことができる効果がある。

4．図面の簡単な説明

第1図は本発明の一実施例に係るマスタスライス方式LSIの配線構造を示す図、

第2図は配線ネットの端子ペアの一例を示す図、

第3図は第1の配線層および第2の配線層を用いた配線処理後の配線例を示す図、

第4図は第3の配線層を用いて人手修正を行った後の配線例を示す図、

第5図は第1の配線層および第2の配線層を用いて人手修正を行った後の配線例を示す図である。

図において、

1・・・第1の配線層、

2・・・第2の配線層、

3・・・第3の配線層、

101，102，221・配線経路、

231，232・スルーホール、

11，12・端子である。

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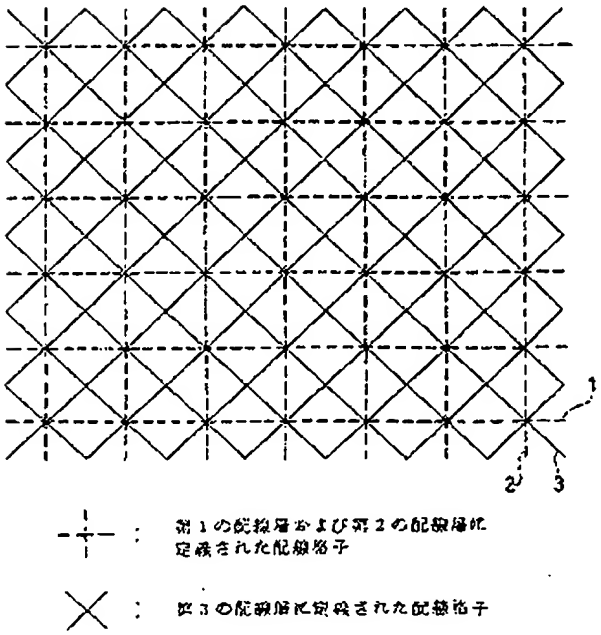
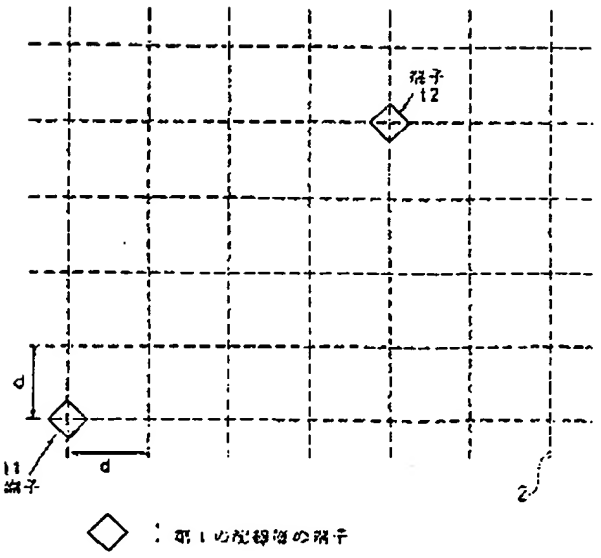
北陸日本電気ソフトウェア株式会社
代理人弁理士　何間純一

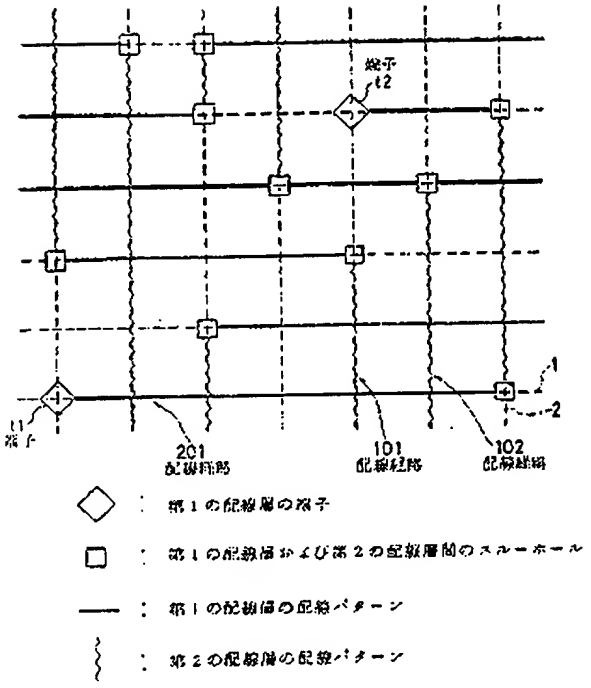
第1図



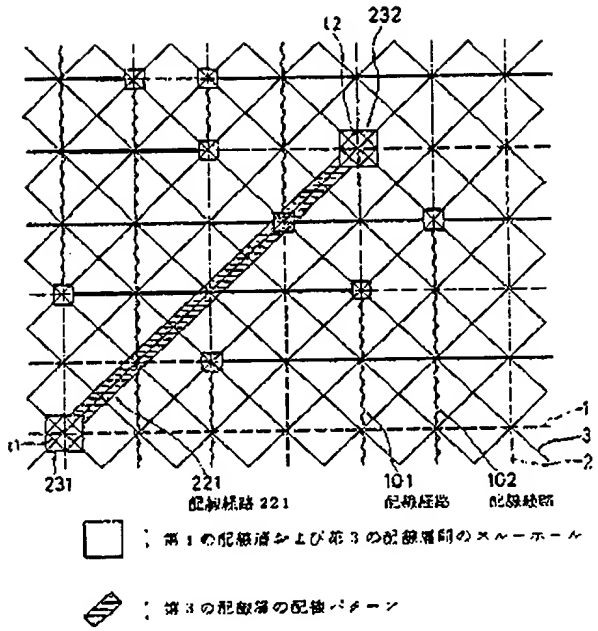
第2図



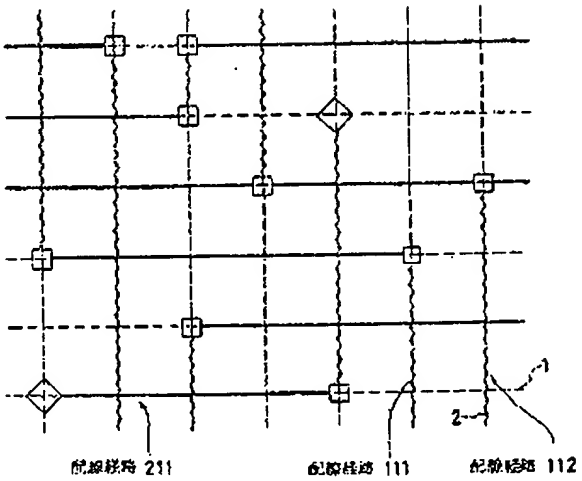
第 3 図



第 4 図



第 5 図



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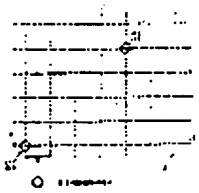
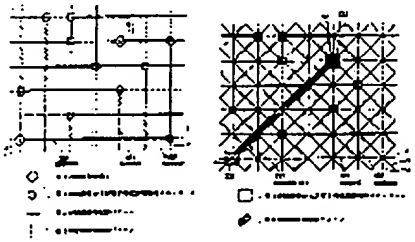
(54) WIRING STRUCTURE OF MASTER SLICE SYSTEM LSI

(57)Abstract:

PURPOSE: To comparatively easily adjust wiring length by arranging a first and a second wiring layer wherein a vertical and a horizontal wiring lattice are defined and a third wiring layer wherein a wiring lattice connecting diagonal lines of both lattices is defined.



CONSTITUTION: When both of the lattice intervals in the vertical and the horizontal directions are (d), the wiring length between the terminals t1 and t2 of a wiring network is shorter than or equal to 8d, in order to satisfy restrictions like the delay time of an LSI required for high speed operation. When wiring process is performed by using a first and a second wiring layer 2 in accordance with the order that the angle of the line connecting the terminals t1 and t2 is approximate to 0° or 90°, the wiring between the terminal t1 and t2 is detoured by wiring routes 101 and 102, and a wiring route 201 of α length 12d is obtained. On the other hand, by constituting an oblique wiring between the terminals t1 and t2 by using the layer 3, a wiring route 221 of a length l=4.22/1d can be obtained as follows, the wiring routes 101 and 102 are not corrected, and through holes 231 and 232 between the first and the this wiring 1, 3 are arranged at the positions of the terminals t1 and t2.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

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[Patent number]

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(43) **KOKAI Date: July 26, 1991**

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Examination Request Status: Not yet requested

Number of Claims: 1 (Total 4 pages [in orig.])

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(54) **Title of Invention**

Master Slice LSI Wiring Structure

(21) **Patent Application No.** H1-312541 [1989]

(22) **Filing Date:** December 1, 1989

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Specification

1. Title of Invention

Master Slice LSI Wiring Structure

2. Claims

A master slice LSI wiring structure comprising:

a first wiring layer and a second wiring layer for which vertical-direction and horizontal-direction wiring lattice members are defined; and

a third wiring layer for which diagonal wiring lattice members are defined which join diagonals of vertical-direction and horizontal-direction lattice points defined in said first wiring layer and second wiring layer.

3. Detailed Description of Invention

[Field of the Invention]

This invention concerns a master slice LSI wiring structure, and more particularly concerns a master slice LSI wiring structure for producing LSIs, wherewith, using common masks prior to the wiring step, only masks pertaining to the wiring are designed and fabricated individually for each product type.

[Prior Art]

Conventionally, in this type of master slice LSI wiring structure, all of the wiring lattice members in the wiring layers are defined in the vertical direction and horizontal direction (cf. "Ronri Sochi no CAD [Logic Device CADs]", Joho Shori Gakkai (Japan Society for Information Processing), March 20, 1981).

A case is now described wherein, as diagrammed in Fig. 2, when both the vertical direction lattice member interval and the horizontal direction lattice member interval are made d, and the wiring length between the terminals t1 and t2 in the wiring network is limited to 8d or less in order to satisfy restrictions such as the LSI delay time required for high-speed operation, as a result of implementing a wiring process that does the wiring using the first wiring layer 1 and the second wiring layer 2 sequentially from an angle of the straight line connecting the terminals t1 and t2 that is near either 0 or 90 degrees, the wiring between the terminals t1 and t2 is made circuitous by wiring paths 101 and 102, as diagrammed in Fig. 3, yielding the wiring path 201 having a wiring length of 12d, whereupon, with the conventional master slice LSI wiring structure, as diagrammed in Fig. 5, the wiring paths 101 and 102 are altered manually to yield wiring paths 111 and 112, whereby the wiring path 211 having a wiring length of 8d which

satisfies the restriction is obtained.

[Problems Which the Present Invention Attempts to Solve]

With the conventional master slice LSI wiring structure described in the foregoing, if, after the wiring process in wiring a wiring net wherein a limitation is placed on the wiring length in order to satisfy a restriction such as the LSI delay time required for high-speed operation, that limitation has not been met, it is necessary to alter the wiring, moving other wiring, in order to satisfy the limitation. Many steps are required for such alteration, which constitutes a shortcoming.

Furthermore, in cases where the wiring length limitation cannot be met even after the wiring has been altered, it is necessary to redo the wiring process, performing block placement alterations, etc., resulting in a further increase in processing time, which is a shortcoming.

In view of these shortcomings, an object of the present invention is to provide a master slice LSI wiring structure wherewith, using a third wiring layer for which diagonal wiring lattice members are defined which join diagonals of vertical-direction and horizontal-direction lattice points defined by the first wiring layer and the second wiring layer, wiring lengths can be adjusted with comparative ease, without moving the other wiring or changing block placement positions.

[Means Used to Solve the Abovementioned Problems]

The master slice LSI wiring structure of the present invention comprises: a first wiring layer and a second wiring layer for which vertical-direction and horizontal-direction wiring lattice members are defined; and a third wiring layer for which diagonal wiring lattice members are defined which join diagonals of vertical-direction and horizontal-direction lattice points defined in the first wiring layer and second wiring layer.

[Operation]

In the master slice LSI wiring structure of the present invention, vertical direction and horizontal direction wiring lattice members are defined in the first wiring layer and the second wiring layer, and diagonal wiring lattice members are defined in the third wiring layer, which diagonal wiring lattice members join the diagonals of the lattice points of the horizontal direction and vertical direction wiring lattice members defined in the first wiring layer and the second wiring layer.

[Embodiments]

The present invention is now described in detail, making reference to the drawings.

Fig. 1 is a diagram of a master slice LSI wiring structure in one embodiment of the present invention. The master slice LSI wiring structure in this embodiment comprises: a first wiring layer and a second wiring layer 2 for which vertical-direction and horizontal-direction

wiring lattice members are defined; and a third wiring layer 3 for which diagonal wiring lattice members are defined which join diagonals of vertical-direction and horizontal-direction lattice points defined in the first wiring layer 1 and second wiring layer 2.

The process of implementing the wiring in the master slice LSI wiring structure in this embodiment, configured as stated, is now described specifically, with reference to Fig. 2 to 4.

The case is [again] described wherein, as diagrammed in Fig. 2, when both the vertical direction lattice member interval and the horizontal direction lattice member interval are made d, and the wiring length between the terminals t1 and t2 in the wiring network is limited to 8d or less in order to satisfy restrictions such as the LSI delay time required for high-speed operation, as a result of implementing a wiring process that does the wiring using the first wiring layer 1 and the second wiring layer 2 sequentially from an angle of the straight line connecting the terminals t1 and t2 that is near either 0 or 90 degrees, the wiring between the terminals t1 and t2 is made circuitous by wiring paths 101 and 102, as diagrammed in Fig. 3, yielding the wiring path 201 having a wiring length of 12d, whereupon, as diagrammed in Fig. 4, without altering the wiring paths 101 and 102, through holes 231 and 232 are opened between the first wiring layer 1 and the third wiring layer 3 at the positions of the terminals t1 and t2, [respectively,] and diagonal wiring is implemented between terminal t1 and terminal t2 using the third wiring layer 3, thereby obtaining a wiring path 221 having a wiring length equal to

$$\ell = \sqrt{(4d)^2 + (4d)^2}$$
$$= 4\sqrt{2}\, d$$

which meets the limitation.

[Benefits of Invention]

After wiring processing has been performed using a first wiring layer and a second wiring layer, and there exists wiring that does not meet a wiring length limitation established to satisfy a restriction such as an LSI delay time required for high-speed operation, the present invention, as described in the foregoing, employs a third wiring layer to make that wiring meet that limitation, thereby making it possible to adjust wiring lengths with comparative ease without moving the other wiring or altering block placement positions.

4. Brief Description of Drawings

Fig. 1 is a diagram of a master slice LSI wiring structure in one embodiment of the present invention;

Fig. 2 is a diagram of one example of a pair of terminals in a wiring network;

Fig. 3 is a diagram of an example of wiring after the implementation of a wiring process using a first wiring layer and a second wiring layer;

Fig. 4 is a diagram of an example of wiring after a manual alteration using a third wiring

layer; and

Fig. 5 is a diagram of an example of wiring after performing a manual alteration using a first wiring layer and a second wiring layer.

The following reference characters are used in the drawings.

1 First wiring layer

2 Second wiring layer

3 Third wiring layer

101, 102, 221 Wiring paths

231, 232 Through holes

t1, t2 Terminals

Patent Applicants NEC Corporation

Hokuriku NEC Software, Ltd.

Agent Junichi Kawahara, patent attorney

Figure 1

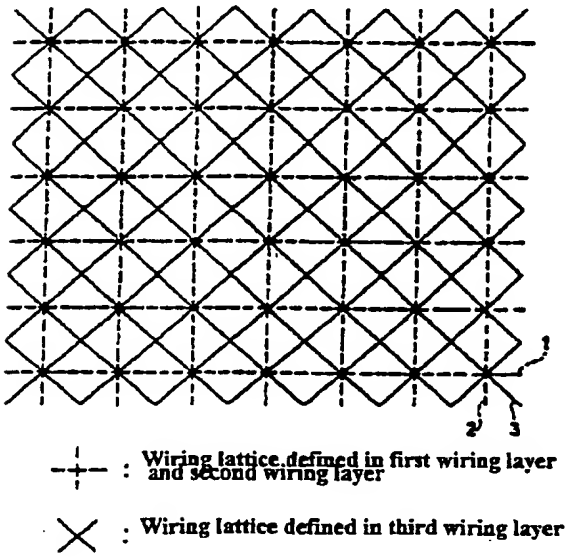


Figure 2

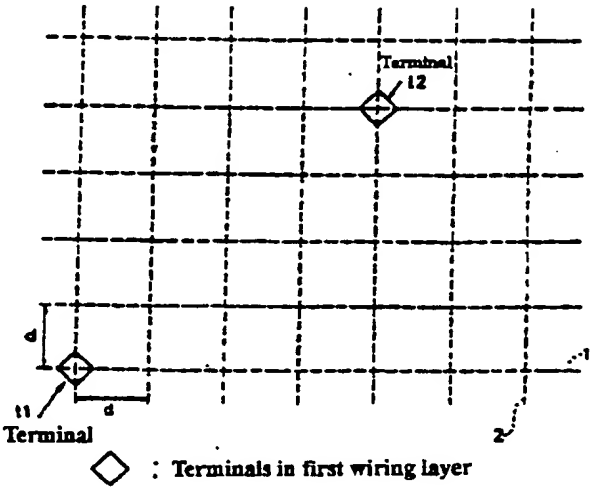


Figure 3

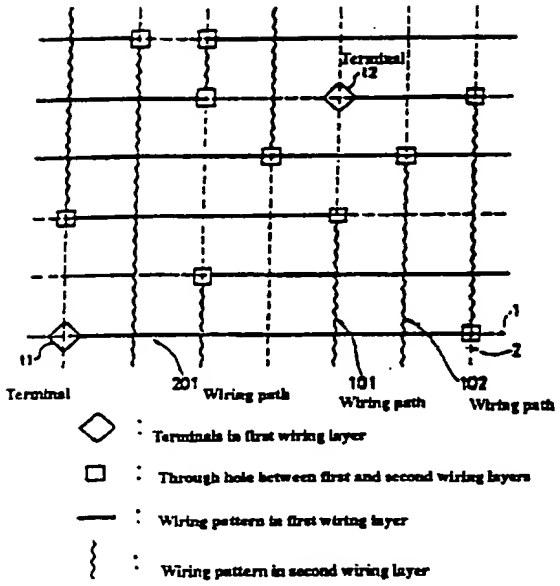


Figure 4

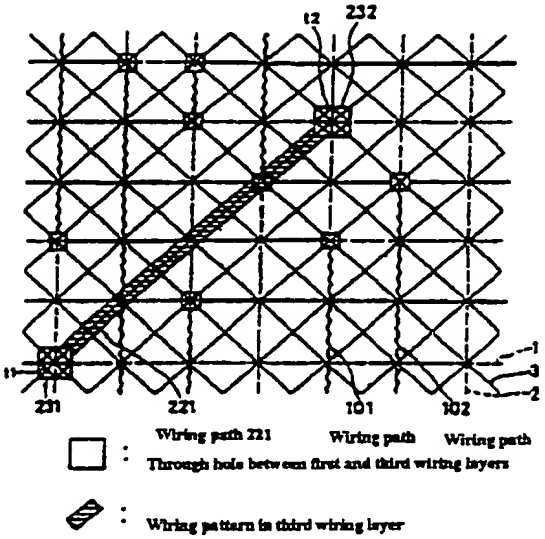
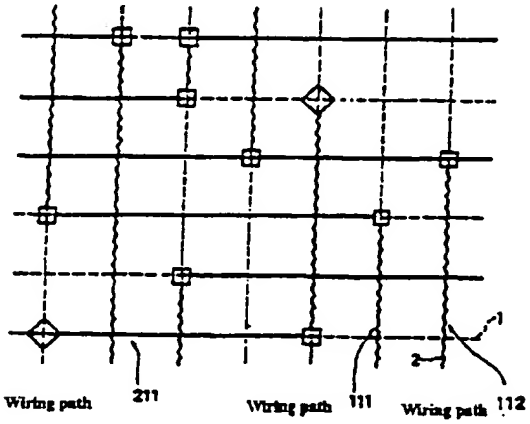


Figure 5



[Translator's Notes]

1. The original term koushi, usually translated "lattice" (and sometimes "grating" or "grid") is herein translated "lattice member" because the English word "lattice" refers to the entire lattice and never to its constituent elements or "members" as is apparently intended here.

2. The term haisen, as used in microchip technology, may also be translated "interconnect," but is translated by the more common "wiring" herein to avoid confusion.

3. The original language [A] ni teigi sareta [B], which occurs frequently in the text, is ambiguous. I have translated it "B defined in A," but it could also mean "B defined by A.